WHAT IS CLAIMED IS:

1. A method of fabricating a semiconductor device, comprising:

providing a layer of high-k dielectric material over a substrate;

providing a layer of conductive material over the high-k dielectric layer;

patterning the conductive layer;

performing a first etch on the high-k dielectric layer, wherein a portion of the high-k dielectric layer being etched with the first etch remains after the first etch;

performing a second etch of the high-k dielectric layer to remove the remaining portion of the high-k dielectric layer, wherein the second etch differs from the first etch.

2. The method of claim 1, wherein the first and second etches of the high-k dielectric layer are performed in alignment with the patterned conductive layer.

3. The method of claim 1, further comprising:

providing spacers along sidewalls of the patterned conductive layer, wherein the first and second etches of the high-k dielectric layer are performed, at least in part, in alignment with the spacers.

4. The method of claim 1, wherein the first etch is a dry etch process.

5. The method of claim 4, wherein the dry etch process is a reactive ion etching process using an etch chemistry comprising at least one of inert gas, chlorine, and fluorine.

6. The method of claim 1, wherein the second etch is a wet etch process.

7. The method of claim 6, wherein the wet etch process uses an etch chemistry comprising an inorganic acid.

8. The method of claim 7, wherein the inorganic acid comprises at least one of a halogen acid, HF, and H_2SO_4.

9. The method of claim 1, wherein the patterning of the conductive layer, the first etch, and the second etch are performed in a same chamber.

10. The method of claim 1, further comprising:

plasma ashing the remaining portion of the high-k dielectric layer after the first etch and before the second etch.

11. The method of claim 1, wherein the high-k dielectric material comprises at least one of an aluminum oxide, a zirconium oxide, a hafnium oxide, a hafnium silicate, a zirconium silicate, a silicon nitride, a tantalum oxide, a barium strontium titanate, and a lead-lanthanum-zirconium-titanate.

12. The method of claim 1, further comprising:

changing material properties of the remaining portion of the high-k dielectric layer during the first etch.

13. The method of claim 1, wherein the high-k dielectric layer is provided using a process selected from a group consisting of chemical vapor deposition, metal-organic chemical vapor deposition, atomic layer deposition, atomic layer chemical vapor deposition, low pressure chemical vapor deposition, sputtering, and anodization.

14. The method of claim 1, wherein the high-k dielectric layer has an initial thickness prior to the first etch, wherein the remaining portion of the high-k dielectric layer has a first thickness after the first etch, the first thickness being about half the initial thickness.

15. A method of fabricating a semiconductor device, comprising:

providing a layer of high-k dielectric material over a substrate;

providing a layer of conductive material over the high-k dielectric layer;

patterning the conductive layer;

performing a dry etch on the high-k dielectric layer, wherein a portion of the high-k dielectric layer being etched with the dry etch remains after the dry etch;

performing a wet etch of the high-k dielectric layer to remove the remaining portion of the high-k dielectric layer.

16. The method of claim 15, further comprising:

plasma ashing the remaining portion of the high-k dielectric layer after the dry etch and before the wet etch.

17. The method of claim 15, wherein the dry and wet etches of the high-k dielectric layer are performed in alignment with the patterned conductive layer.

18. The method of claim 15, further comprising:

providing spacers along sidewalls of the patterned conductive layer, wherein the dry and wet etches of the high-k dielectric layer are performed, at least in part, in alignment with the spacers.

19. The method of claim 15, further comprising:

changing material properties of the remaining portion of the high-k dielectric layer during the dry etch.

20. A method of patterning a layer of high-k dielectric material, comprising:

performing a first etch on the high-k dielectric layer, wherein a portion of the high-k dielectric layer being etched with the first etch remains after the first etch;

performing a second etch of the high-k dielectric layer to remove the remaining portion of the high-k dielectric layer, wherein the second etch differs from the first etch.

21. The method of claim 20, wherein the first etch is a dry etch process, and wherein the second etch is a wet etch process.

22. The method of claim 20, further comprising:

plasma ashing the remaining portion of the high-k dielectric layer after the first etch and before the second etch.